P/N:YZPST-RGN100C066

100V Super-GaN FET

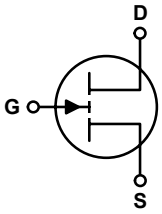
100V, 230A, 3.2mΩ, Super-GaN FET in WLCSP 3.5x2.13

Features

GaN-on-Silicon E-mode HEMT technology
Very low gate charge
Ultra-low on resistance
Very small package size
Zero reverse recovery charge

Applications

Synchronous rectification
Class-D audio
High frequency DC-DC converter
Communication base station
Motor driver



Pin information

PIN	Pin Description	Pin Function
2,4,6,8	Source	Power Source
3,5,7	Drain	Power Drain
1	Gate	Driver Gate

Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	100	V
$R_{DS(on),max}$ @ V_{GS} = 5 V	3.2	mΩ
$Q_{G,typ}$ @ V_{DS} = 50V	9.2	nC
$I_{DS,Pulse}$	230	A
Q_{OSS}@ V_{DS} = 50V	50	nC

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Maximum ratings at T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
I_D	Continuous current	60	A
	Pulsed (25˚C, T_{PULSE} = 300 μs)	230	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	˚C

Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.3	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.5	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [1]	33	˚C/W

Electric characteristics at T_j = 25 °C unless otherwise specified.

Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Voltage	100	-	-	V	V_{GS} = 0 V, I_D = 400 μA
I_{DSS}	Drain Source Leakage	-	4	28	μA	V_{GS} = 0 V, V_{DS} =80 V
I_{GSS}	Gate-to-Source Forward Leakage(25°C)	-	1.2	23	μA	V_{GS} = 5 V
	Gate-to-Source Forward Leakage(125°C)		0.1	2	mA	V_{GS} = 5 V
	Gate-to-Source Reverse Leakage	-	0.1	0.5	μA	V_{GS} = -4 V
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.1	2.5	V	V_{DS} = V_{GS}, I_D = 9 mA
$R_{DS(on)}$	Drain-Source On-state Resistance	-	2.5	3.2	mΩ	V_{GS} = 5 V, I_D = 25 A
V_{SD}	Source-Drain Forward Voltage	-	1.5	-	V	I_S = 0.5 A, V_{GS} = 0 V

Dynamic characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance	-	1000	-	pF	V_{GS} = 0 V, V_{DS} = 50 V
C_{OSS}	Output Capacitance	-	460	-		V_{GS} = 0 V, V_{DS} = 50 V
C_{RSS}	Reverse Transfer Capacitance	-	8.2	-		V_{GS} = 0 V, V_{DS} = 50 V
$C_{OSS(ER)}$	Energy Related C_{OSS}	-	700	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
$C_{OSS(TR)}$	Time Related C_{OSS}	-	1020	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
R_G	Gate resistance	-	2.2	-	Ω	f = 5 MHz, open drain
Q_G	Total Gate Charge [1]	-	9.2	12	nC	V_{GS} = 5 V, V_{DS} = 50 V, I_D= 25 A
Q_{GS}	Gate to Source Charge	-	1.9	-		V_{DS} = 0 V to 50 V, I_D = 25 A
Q_{GD}	Gate to Drain Charge	-	1.7	-		V_{DS} = 0 V to 50 V, I_D = 25 A
$Q_{G(TH)}$	Gate Charge at Threshold	-	1.1	-		V_{DS} = 0 V to 50 V, I_D = 25 A
Q_{OSS}	Output Charge	-	**50**	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V

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Electric characteristics diagrams at T_j = 25 °C unless otherwise specified.

Fig. 1 Typical Output Characteristics (T_J=25°C)

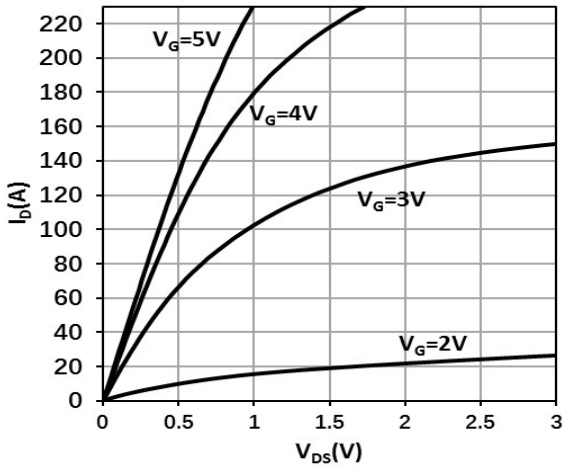

Fig. 2 Typical Output Characteristics (T_J=125°C)

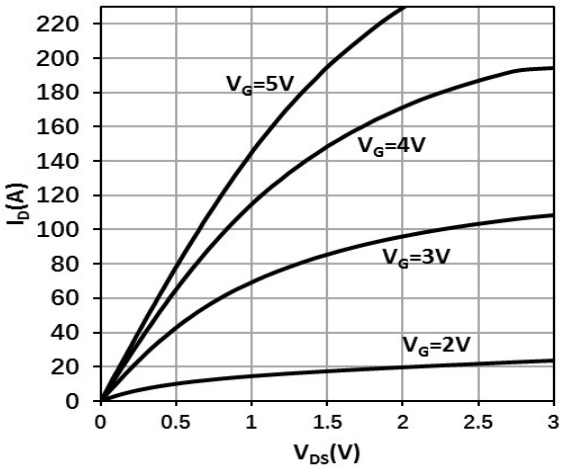

Fig. 3 Typical Drain On-state Resistance (T_J=25°C)

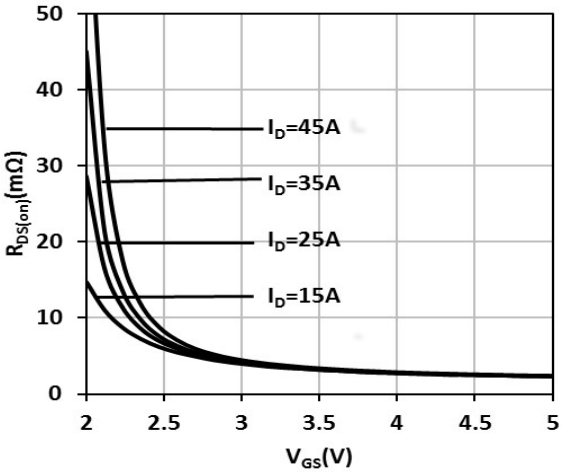

Fig. 4 Typical Drain On-state Resistance (T_J=125°C)

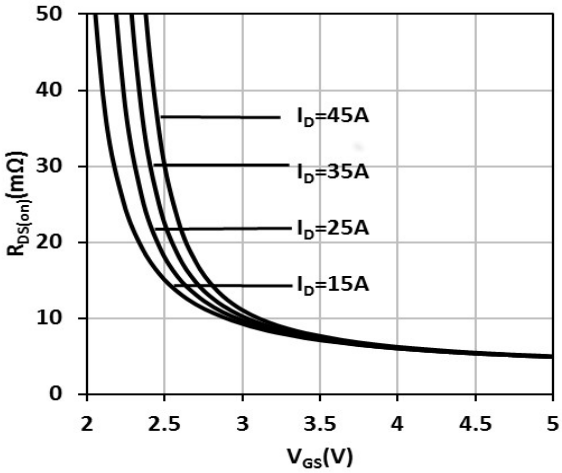

Fig. 5 Normalized On-State Resistance vs. Temp.

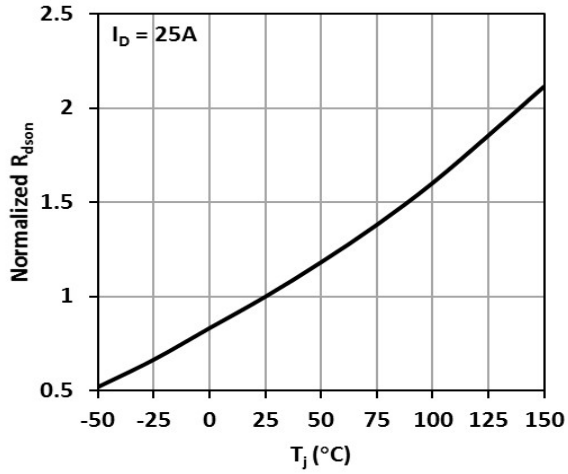

Fig. 6 Typical Transfer Characteristics

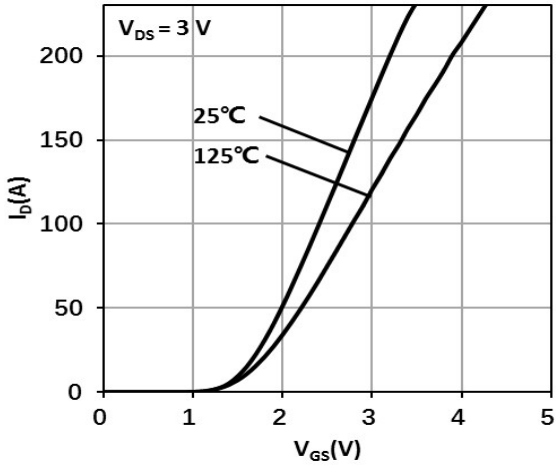

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Fig. 7 Typ. Reverse Drain-Source Characteristics ($V_{GS}\leqslant 0, T_J=25°C$)

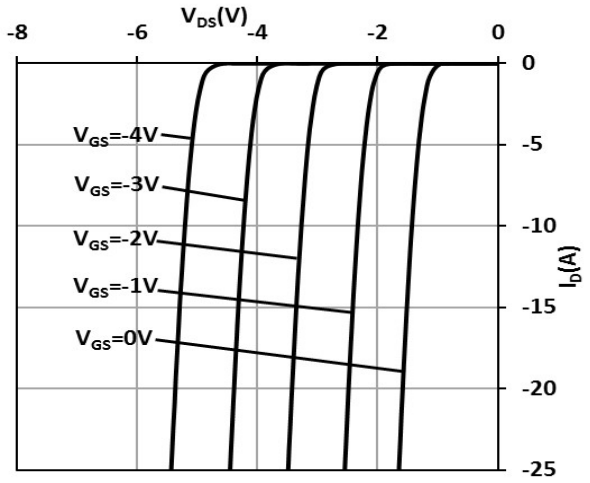


Fig. 8 Typ. Reverse Drain-Source Characteristics ($V_{GS}\geqslant 0, T_J=25°C$)

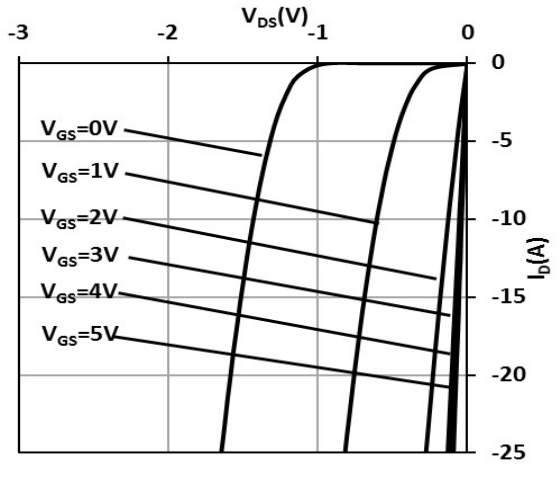


Fig. 9 Typ. Reverse Drain-Source Characteristics ($V_{GS}\leqslant 0$, $T_J=125°C$)

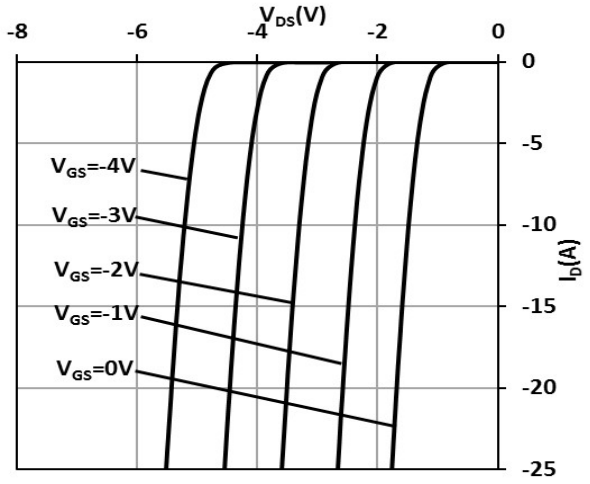


Fig. 10 Typ. Reverse Drain-Source Characteristics ($V_{GS}\geqslant 0$, $T_J=125°C$)

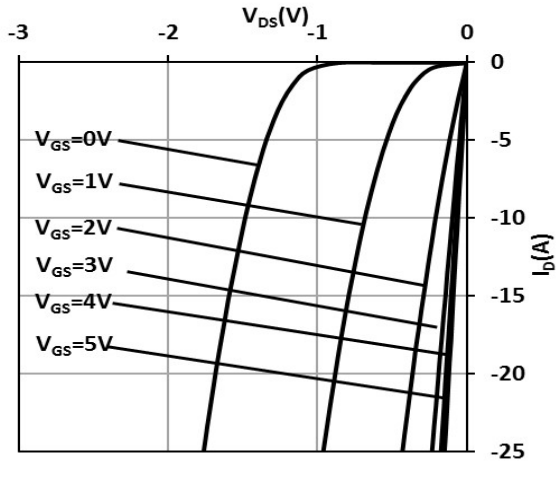


Fig. 11 Typ. Capacitances Characteristics

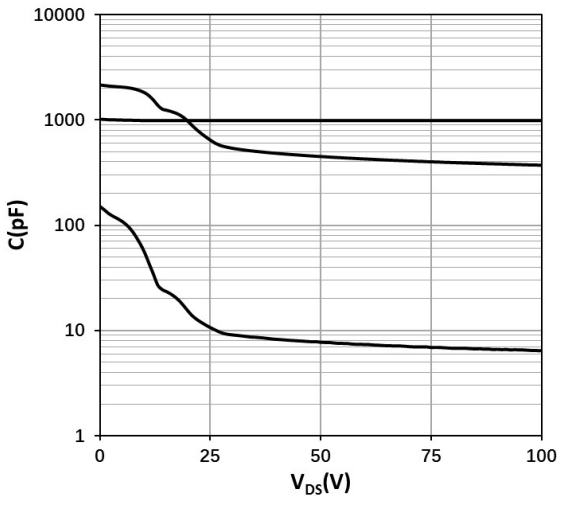


Fig. 12 Typ. Gate Charge

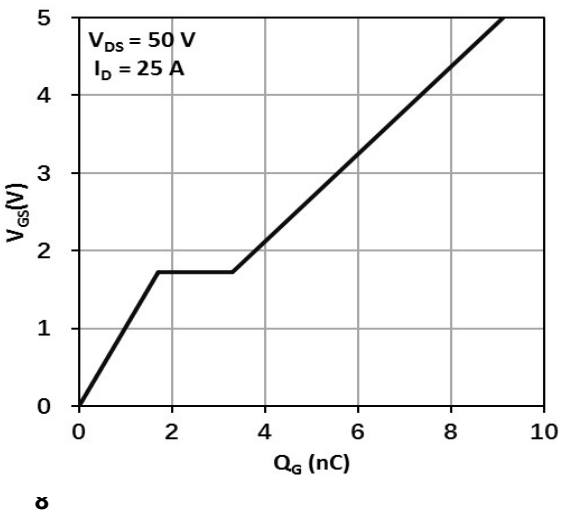


Fig. 13 Normalized Threshold Voltage vs. Temp.

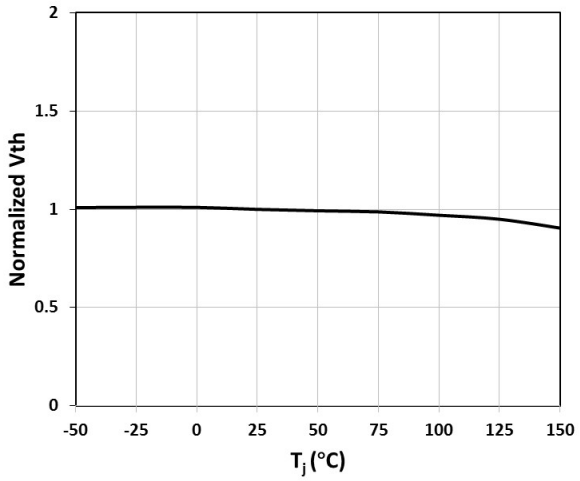


Fig. 14 Output Charge

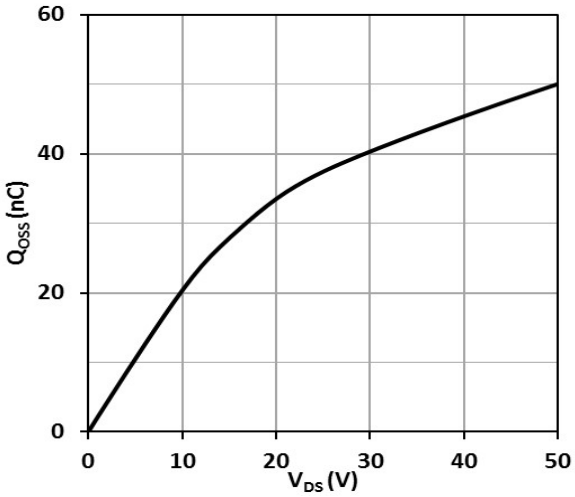


Fig. 15 Output Capacitance Stored Energy

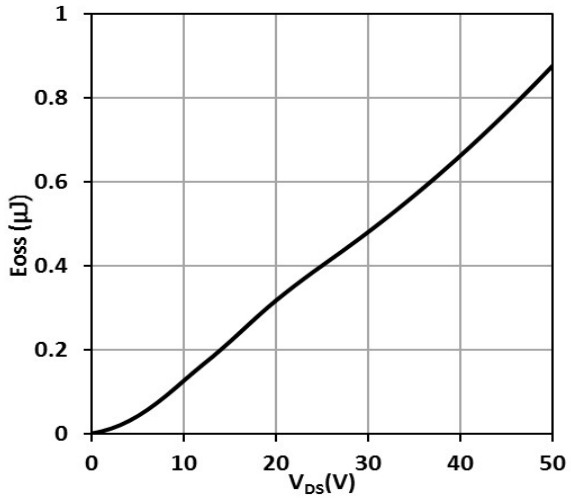


Fig. 16 Power Dissipation

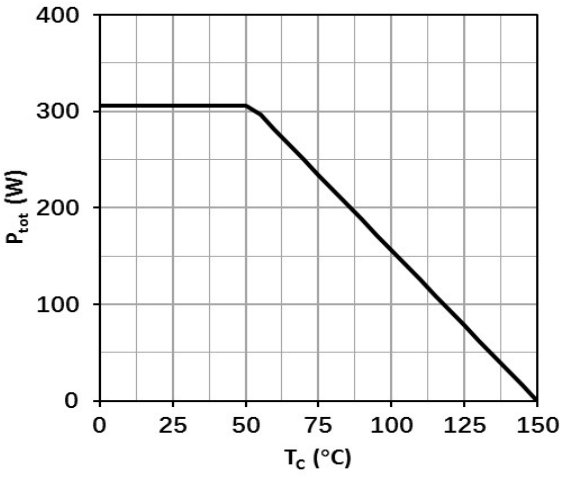


Fig. 17 Safe Operating Area

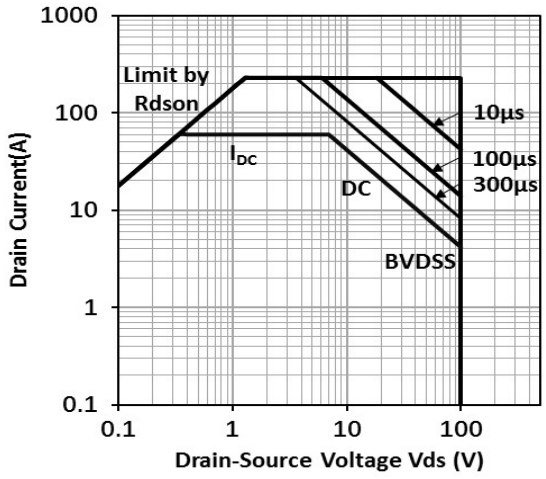
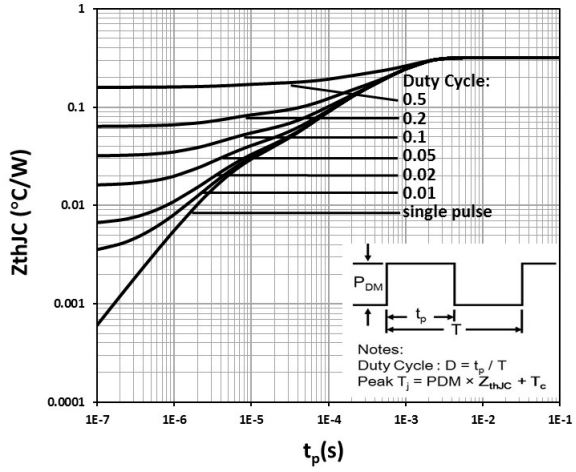
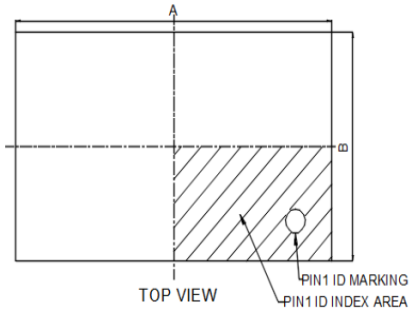
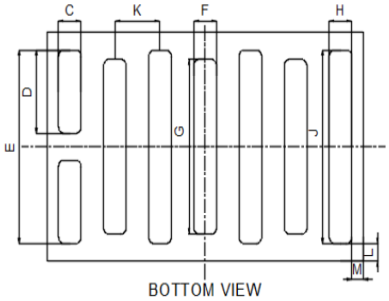


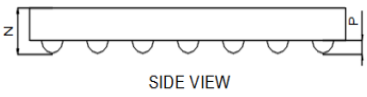
Fig. 18 Max. Transient Thermal Impedance



Package Reference





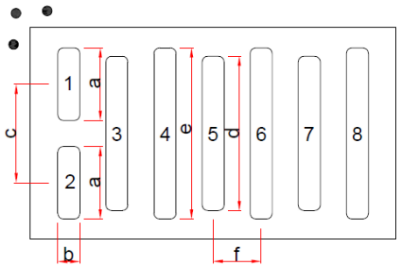


NOTE:
1)ALL DIMENSION ARE IN MILLIMETERS.
2)BOTTOM VIEW IS SOLDER BAR VIEW.
3)COMPLIES WITH JEDEC MO-211.
4)DRAWING IS NOT TO SCALE.
5)A,B IS PACKAGE SIZE
6)BAR COPLANARITY SHALL BE 0.05 MILLMETERS MAX

SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	3.475	3.5	3.525	
B	2.105	2.13	2.155	
C	0.23	0.25	0.27	2X
D	0.755	0.775	0.795	2X
E	1.78	1.8	1.82	
F	0.23	0.25	0.27	3X
G	1.605	1.625	1.645	3X
H	0.23	0.25	0.27	3X
J	1.78	1.8	1.82	3X
K	0.5 BASIC			7X
L	0.165 REF			
M	0.125 REF			
N	0.394	0.429	0.464	
P	0.1	0.12	0.14	

Land Pattern

Recommended Land Pattern
Top View

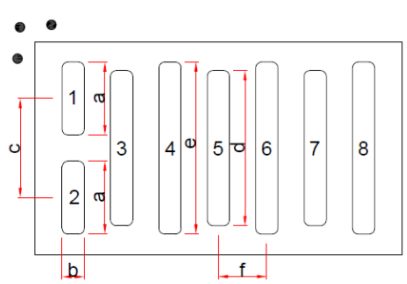


Land pattern is solder mask defined
Solder mask opening is 0.23mm
It is recommended to have on-Cu trace PCB vias

DIM	Millimeter
a	0.775
b	0.250
c	1.025
d	1.605
e	1.780
f	0.500

Pad 1 is Gate;
Pads 2 ,4, 6, 8 are Source;
Pads 3, 5, 7 are Drain;

Recommended Stencil Drawling
Top View



DIM	Millimeter
a	0.775
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